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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,462	10/20/2003	Wen-Ting Chu	N1085-00156	4151

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DUANE MORRIS LLP  
IP DEPARTMENT (TSMC)  
30 SOUTH 17TH STREET  
PHILADELPHIA, PA 19103-4196

EXAMINER
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WARREN, MATTHEW E

ART UNIT	PAPER NUMBER
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2815

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/689,462	<b>Applicant(s)</b> CHU ET AL.	
	<b>Examiner</b> Matthew E. Warren	<b>Art Unit</b> 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 November 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-13 and 34-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 34-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on November 30, 2006.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6-8, 34, 36, 37, 39, and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Chern (US 6,563,167).

In re claims 1, 36, 39, and 40, Chern discloses (figs. 3E-3M) a method of forming a split gate field effect transistor comprising: providing a substrate (10) having a pair of floating gate portions (14), a first conductive material layer (36) between the pair of floating gate layer portions, and a first dielectric layer (38) above said first conductive material layer; forming a pair of floating gates (14, fig. 3H) from said pair of floating gate layer portions using the first dielectric layer (38) as a first etching hard mask; forming a substantially rectangular control gate (54, fig. 3L) (read col. 8, line 67-col. 9, line 1) having a second dielectric layer (50) above said control gate (46, fig. 3K), wherein said control gate is self-aligned to said pair of floating gates by using said first and second

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dielectric layer as a second etching hard mask (col. 2, lines 7-17); and forming a pair of source/drain regions (60, fig. 3M) into the substrate and beside the pair of floating gates and said control gate.

In re claims 2-4 and 34 Chern discloses (col. 6, lines 52-67 and col. 7, lines 28-37) that the first (38) and second dielectric (50) layers comprise a silicon oxide layer. The second dielectric layer is formed by thermal oxidation. The silicon oxide layer (50) has a minimum thickness of 80 angstroms (8nm), which fits within the range recited in claim 4.

In re claims 6-8 and 37, Chern discloses (figs. 3I-3L and col. 7, lines 7-37) that the step of forming the control gate comprises: forming a second conductive material layer (46) above the substrate; forming a hard mask layer (48) above said second conductive material layer; removing portions of said hard mask layer and said second conductive material layer (fig. 3J); and removing a remaining portion of said hard mask layer and an addition portion of said conductive material layer (fig. 3L) by using said first dielectric layer (38) and said second dielectric layer (50) as said second etching hard mask. The second dielectric layer (50) is formed by using said hard mask layer as an oxidation resistant layer, and the hard mask layer comprises silicon nitride (col. 7, lines 7-13).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 9-13, 35, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chern (US 6,563,167) as applied to claims 1, 6, and 37 above, and further in view of Ryu et al. (US 6,800,525 B2).

In re claim 5, Chern shows all of the elements of the claims except the second dielectric layer being thicker in the middle than at an edge portion. Ryu shows (fig. 2k) that a second dielectric layer (217) formed on the control gate portion (214b) is thicker in the middle than at an edge portion. With such a configuration, the conductive material under the mask in the middle of the mask has adequate protection. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second dielectric layer of Chern by forming the second dielectric being thicker than at the edges as taught by Ryu to provide adequate protection to the underlying conductive material layer.

In re claims 9-13 and 38, Chern shows all of the elements of the claims except the step of removing portions of the hard mask layer and second conductive material layer comprising forming a sacrificial layer. Ryu discloses (fig. 2g) that a sacrificial layer (216) is formed above the hard mask layer (215). The method also includes removing portions of the sacrificial layer (216), the hard mask layer (215) and the second conductive layer (214) (fig. 2h). A remaining portion of the sacrificial layer is also removed (fig. 2k). By forming a sacrificial layer over the substrate, step coverage throughout the entire substrate is improved during the planarization process (col. 5,

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lines 1-13). The sacrificial layer (216) is used to planarize the surface of the substrate (fig. 2i). The sacrificial layer may be an HDP-CVD film (organic), which may function as a photoresist, or a USG (spin on glass) layer (col. 5, lines 9-12). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Chern by adding a sacrificial layer as taught by Ryu to improve the step coverage across the entire substrate during a planarization process.

In re claim 35, Chern discloses that the second dielectric has a thickness in the desired range but does not disclose what the thickness of the first dielectric is. it would have been obvious to one of ordinary skill in the art to make the thickness of the first dielectric within the desired range, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. In this case, one of ordinary skill in the art would be motivated to form the dielectric having a desired thickness to provide adequate protection during the etching process.

### ***Response to Arguments***

Applicant's arguments filed with respect to claims 1-13 and 34-40 have been fully considered but they are not persuasive. The applicant primarily argues that the prior art references do not show all of the elements of the claims, specifically that Chern does not show the amended limitation of the control gate having a substantially rectangular shape. As stated in the rejection above and despite what the figures show, Chern discloses (read col. 8, line 67-col. 9, line 1) that the control gate (54) has a generally

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rectangular shape. Therefore, Chern shows all of the elements of the claims and the rejection is proper.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew E. Warren



December 11, 2006